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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN BA, HOANG VU A	
ART UNIT	**PAPER NUMBER**
2623	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/083,351	HOSOKAWA, NOBORU	
	Examiner	Art Unit	
	Hoang-Vu A. Nguyen-Ba	2623	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 26, 2007 has been entered.

2. Claims 1-9 remain pending. Claim 1 is an independent claim.

Response to Amendments

3. Per Applicant's request, Claim 1 has been amended.

Response to Argument

4. Applicant's arguments in the Remarks, filed concurrently with the RCE, have been fully considered but are not moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,683,642 to Kobayashi et al. ("Kobayashi") in view of admitted prior art (APA) of pages 1-3 of Applicant's background.

Claim 1

Koyabashi discloses at least:

a central processing unit block (see at least FIG. 1, component 68a)*; and*

a peripheral block (see at least FIG. 1, all the components to the left of Bus Bridge 64, *wherein said peripheral block includes a video processing unit for processing video signals* (see at least FIG. 1, components 18 and 26 in conjunction with components 16, 20a-d, 22a-d, 24, 26, 32, 28, 62, 58) *from an image picking-up device* (see at least FIG. 1, component 12 in conjunction with components 13-15) *and generating video data, and*

a first bus (see at least FIG. 1, bus 30 connecting the block of components 62- 60-58 with Bus Bridge 64)*;*

wherein said central processing unit block includes a central processing unit for processing said video data (see at least FIG. 1, component 68a)*, a storage unit for storing video data from said video processing unit* (see at least FIG. 1, DRAM 70; it should be noted that SDRAM 34 can substitute for DRAM 70 as suggested by Koyabashi at 11:32-38)*, a central control unit for controlling said video processing unit, said network control unit and said storage unit in cooperation with said central processing unit* (see at least FIG. 1, component 32)*, and*

a second bus for providing a series connection of said central processing unit, said storage unit and said central control unit (see at least FIG. 1, bus 66), *and*

wherein said first bus and said second bus are connected through a first bus buffer (see at least FIG. 1, bus 66 and bus 30 are connected in series through Bus Bridge 64).

Kobayashi does not specifically disclose *a network control unit for controlling transmission and reception of said video data transmitted and received through a transmission medium inclusive of a network* and that the first bus *provid[es] a series connection without any branch of said video processing unit and said network control unit.*

However, the network control unit and its functions are disclosed in Applicant's background at p.1, lines 7-22 and p. 2, lines 11-16.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to add this unit to Kobayashi at a location between blocks 62-60-58 and the Bus Bridge 64, as this would allow Kobayashi video data to be communicated with a network and a central control unit (e.g., using DMA transmission function) as described in Applicant's background at page 1.

It should be further noted that in light of FIG. 3 of Applicant's disclosure:

1. the components claimed in the claim (i.e., CPU 1, storage unit interpreted as RAM 3 + ROM 5, central control 4, first buffer 2, network control 7, JPEG Enc 8) are physically disposed on the circuit board one following the other in a certain order and this order is not explicitly claimed in the claim and should not be read into the claim;

2. the manner the component are shown as being connected in FIG. 3 of Applicant's disclosure can be interpreted that these devices are being daisy-chained

rather than connected in series, or in a series connection, as defined in the specification or as commonly understood in the art (i.e., the conductor enters a device at one end and exits the same device at another end or in alternatively stated, the device has to process the input data/signal and output the result to the next device); an example of a series connection is shown in FIG. 3 of Applicant's disclosure is the Resistors 23;

3. the use of the language "in series" and " a series connection" can be misleading; and

4. the claimed "bus buffer" and the layout of the components starting from one component in a center of a chip and spiraling out to the edge of the chip may be already known, patented and commercially available (see the HD74LVVC245 product mentioned in Applicant's disclosure at page 29, lines 13-15).

Claim 2

The combination Kobayashi-APA further discloses *wherein said central processing unit and said central control unit control said video processing unit, process the video signals from said image picking-up device and store the compressed video signals in a cycle of 1/30 fps and at a data transmission rate of at least 3.6 Mbps in said storage unit through said first bus, said first bus buffer and said second bus* (see at least APA; p. 2, lines 2-16; it is noted that storing data at a rate of 1/30 fps and transmitting data at a rate of 3.6 Mbps through the bus appear to be admitted by Applicants as known in the art since Applicants claim in their disclosure that their system can transmit twice as fast as 3.6 Mbps (i.e., 7.2 Mbps at p. 9, line 21).

Claim 3

The combination Kobayashi-APA does not specifically disclose *wherein said central processing unit and said control unit read out said compressed video data from said storage unit at a data transmission rate of at least 14.4 Mbps for a request of four users from said network control unit, and transmit said compressed video data to said network control unit through said second bus, said first bus buffer and said first bus.* However, this feature is deemed inherent to APA because of the following reasons:

APA discloses at p. 3, lines 8-15 that using a plurality of DMA transmission functions for executing data access with a built-in buffer and with external equipment independently of command execution of CPU itself and a plurality of interfaces for exchanging data by using the DMA transmission functions under the state where no processing load is applied to CPU itself; and

since the read out function is not *per se* one that requires the processing of the CPU

a simultaneous request of 4 users (3.6 Mbps/each * 4 = 14.4 Mbps) requiring 14.4 Mbps is deemed inherent to the circuit design incorporating a plurality of DAM transmission functions (e.g., 4 buffers).

Claim 7

The combination Kobayashi-APA does not specifically disclose *wherein said first bus further provides a series connection of a circuit for displaying an operating condition of said video transmission apparatus and a switch circuit for setting an operation of said video transmission apparatus.* However, these features are deemed inherent to APA because as discussed at p. 3, lines 16-27 of Applicant's background: 1) a CPU can connect to a JPEG

compression circuit **or** a network control circuit; and 2) the aforementioned connection can be implemented through an interface; it is understood that there must be provided a switch in order to select either the JPEG compression circuit or the network control circuit and thus the switching function could be shown via the interface as to which connection is under operation. Without these inherent features, the system is inoperative.

7. Claims 4-6 and 8-9 are rejected under 35 U.S.C. § 103(a) as being obvious over the combination Kobayashi-APA.

Claim 4

The combination Kobayashi-APA does not specifically disclose *wherein a second bus buffer is further connected in series to said second bus, and a third bus having expansion connectors connected thereto is connected to said second bus buffer.* However, the combination Kobayashi-APA teaches how to use the Bus Bridge 64 to connect Bus 66 and Bus 30 in order to allow data processing with efficiency (see at least FIG. 3).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use similar bus bridge(s) to connect expansion circuit(s) that is similar to the circuit starting with Buffer 36 and ending with Monitor 56 (see at least Koyabashi; FIG. 1, buffer 36 and the downstream circuit) to Bus 30, as taught by the combination Kobayashi-APA in order to allow data processing with efficiency.

Claim 5

The modified combination Kobayashi-APA further discloses *wherein a video expansion unit is connected in series to said expansion connectors of said third bus, and a monitor is connected to said video expansion unit* (see at least FIG. 3, Monitor 56).

Claim 6

The combination Kobayashi-APA does not specifically disclose *wherein said second bus provided to said central processing block unit connects said central processing unit, said storage unit, said central control unit and said first bus buffer in order named, and said first bus provided to said peripheral block connects said first bus buffer, said network control unit and said video processing unit in order named.* However, APA does disclose that in order to conduct data transmission operations at a high speed, some video apparatuses employ a plurality of dedicated bus systems and that such systems enable CPU to simultaneously and independently exchange data with the JPEG compression circuit and with the network control circuit.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify such a system such that these dedicated bus could be named in order. One of ordinary skill in the art would have been motivated to do so for the purpose of facilitating the installation and the troubleshooting of additional dedicated bus systems. See comments in Claim 1.

Claim 8

The combination Kobayashi-APA does not specifically disclose *wherein a dumping resistor is connected to a starting point or an end point of each of said first and second buses and a terminating resistor is connected to the other.* However, Official notice is taken that

dumping resistor is well known in the art to be used for the purpose of matching the characteristic impedance of two circuits on a wiring board and terminating resistor is well known in the art to be used in wiring board for the purpose of minimizing the deterioration of signal qualities without changing the constitution of a semi-conductor unit (e.g., Abstract of JP 2002124775 A).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use dumping and terminating resistors in the combination Kobayashi-APA when connecting additional bus for the purposes discussed above.

Claim 9

The combination Kobayashi-APA does not specifically disclose *wherein said peripheral block and said central processing unit block are arranged on the same packaging board, said central processing unit and said central control unit are positioned at said central processing unit block which is located at a substantial center of said packaging board, and said peripheral block is disposed at a peripheral area of said central processing unit block of said packaging board.*

However, the positioning of the CPU and control unit at the center of circuit board is considered to be a matter of design choice for the purpose of providing the circuit with expansion capability by leaving the outer layer of the circuit board available for connection with add-on circuits and by minimizing the distance from the CPU and control unit to theses add-on circuits by the virtue of the CPU and control unit being at the center location on the circuit board.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate the aforementioned design choice in the list of choices available in APA for the purposes discussed above.

See comments in Claim 1.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Vu "Antony" Nguyen-Ba whose telephone number is (571) 272-3701. The examiner can normally be reached on Tuesday-Friday from 7:00 am to 5:30 pm.

If attempts to reach the examiner are unsuccessful, the examiner's supervisor, John Miller can be reached at (571) 272-7353.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2600 Group receptionist (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

Hoang-vu Antony Nguyen-Ba

January 30, 2008

ANTONY NGUYEN-BA
PRIMARY EXAMINER
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